REMARKS

The Examiner is thanked for the continued indication that claims 3 and 14 define allowable subject matter. The Office Action, however, has continued to reject all remaining claims.

Discussion of Rejections Under 35 U.S.C. § 112, First Paragraph

The Office Action rejected all claims under 35 U.S.C. § 112, first paragraph. In this regard, the Examiner stated that the claimed subject matter was not supported by the specification, and that the previous amendments to claims 1, 11, and 20 were not supported by the specification. Applicant continues to disagree. However, rather than continue to argue this point, Applicant has amended independent claims 1 and 11 to more closely parallel the language of the specification in paragraph 0018 (p. 6, lines 7-23). Accordingly, the rejection under 35 U.S.C. § 112, first paragraph has been rendered moot.

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

The Office Action continued to reject all claims under 35 U.S.C. § 112, second paragraph for various, stated reasons. Applicants respectfully submit that each of these rejections should be withdrawn.

The Office Action rejected claim 20 stating that the language "comprises a plurality of signal of signal lines of the system bus" is unclear. Applicant, however, believes that this issues was corrected in Applicant's previous response, (and therefore is no longer applicable).

The Office Action also stated that the language "collectively, the conductive pins of the integrated circuit component …" is unclear. Applicants have amended this claim element to address and overcome the rejection. By way of further explanation, as will be appreciate by persons skilled in the art, an integrated circuit has conductive pins that couples the semiconductor device to electrical signal lines. Relevantly, a system bus is comprised of a plurality of related signals (e.g., signal lines of a data bus). The claim language specifies that the conductive pins that are on an integrated circuit cannot accommodate all of the signal lines of the system bus. For example, supposed a system bus included 64 signal lines, the integrated circuit may comprise pins for only directly connecting to 32 of the system bus signal lines. In short, Applicant submits that the claim is fully compliant with all statutory requirements.

The Office Action then rejected all claims under 35 U.S.C. § 112, second paragraph, alleging that "essential structure cooperative relationships between elements in the claims … have been omitted." In support of this rejection, the Office Action cites MPEP 2172.01 (Unclaimed Essential Subject Matter), and states that "MPEP 2172.01 requires that relationships between elements recited in claims must be specified." This reflects a misunderstanding of MPEP 2172.01. In fact, MPEP 2172.01 specifically states:

> … *Ex parte Nolden*, 149 U.S.P.Q. 378, 380 (Bd. Pat. App. 1965)("It is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 U.S.P.Q. 447, 448-449 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly

functionally related, do not directly intercooperate, and/or serve independent purposes.

Thus, MPEP 2172 states just the opposite of what the Office Action appears to allege.

On page 13 of the previous Office Action, the Examiner stated: "the word(s) – connected—or –operatively connected— may be used to provide essential structural cooperative relationships between structural elements recited in the claims." Applicant has accepted this suggestion by the Examiner and has amended independent claims 1 and 11 accordingly. Accordingly, these rejections of independent claims 1 and 11 have been rendered moot.

Applicant does not believe that this language is necessary or appropriate for independent claim 20. In view of the foregoing, Applicants respectfully submit that all claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants respectfully request that the rejections thereof be reconsidered and withdrawn.

Discussion of Rejections Under 35 U.S.C. § 102

On a substantive basis, the Office Action rejected the independent claims (claims 1, 11, and 20) under 35 U.S.C. § 102 as allegedly anticipated by U.S. Patent 6,172,906 (hereafter the '906 patent). For at least the reasons set forth herein, Applicants respectfully request reconsideration of the rejections.

With regard to claim 1, claim 1 recites:

> 1. An integrated circuit component comprising:
> logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises only approximately half of a set of signal lines that comprise a system bus; and

> ***logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a remaining portion of the system bus not included in the first portion, wherein the logic capable of being configured to interface with the first portion of the system bus is operatively connected with the logic capable of being configured to interface with the companion integrated circuit.***

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 is directed to "an integrated circuit component" (*i.e.*, a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist the Examiner in a better understanding of claim 1, consider the embodiment of Fig. 2 of the present application. The integrated circuit corresponds to reference numeral 210, while the companion integrated circuit corresponds to reference numeral 211. The first-recited logic element corresponds to split bus logic 214 of integrated circuit 210, while the second-recited logic element corresponds to split bus logic 215 of integrated circuit 210. As is illustrated in Fig. 2, and more particularly claimed in claim 1, the first-recited logic element (e.g., split bus logic 214) is capable of being

configured to interface with a first portion of the system bus 105. Likewise, the second-recited logic (e.g., split bus logic 215) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed through the companion integrated circuit 211. Similarly, claim 1 also covers the embodiment of Fig. 5.

As previously noted by Applicants, the teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1.

The Office Action responded to this previous argument by citing FIGs. 1 and 6. It appears that the Examiner is treating the reference number 600 (of the '906 patent) in FIG. 6a, for example, as denoting a chip. However, it instead denotes an entire memory system. The specification of the '906 patent confirms this (see col. 6, line 36 and col. 7, lines 47-52). Indeed, the Office Action (p. 15) states:

> Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

This position reflects at least one fundamental misapplication of Estakhri to claim 1. As set forth above, reference number 600 (of Fig. 6a) denotes a "memory system" (col. 6, line 36), and not a single integrated circuit. Reference number 506 denotes a "memory bank" (col. 6, line 57), and not a single integrated circuit. Finally, by the Examiner's own admission that reference number 670 comprises a first integrated circuit and reference number 672 comprises a second integrated circuit, the two separate integrated circuits cannot properly/logically comprise a single integrated circuit chip, as expressly claimed by claim 1.

In addition, lines 1-9 of col. 7 of the '906 patent actually state:

> Memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652. Flash bus 675 includes 16 bit lines, 8 bit lines of which form a first bus 680 connected to a port 682 of I/O register 671 of the first flash memory chip, and another 8 bit lines of which form a second bus 684 connected to a port 686 of I/O register 673 of the second flash memory chip.

Even accepting the interpretation of the '906 patent (as applied by the Office Action), the disclosure still fails to teach the claimed features. In this regard, assuming the sections 680 and 682 of the data bus comprises the claimed first and second plurality of signal lines, the memory chips 670 and 672 do not fulfill or provide the requisite features of claim 1. In this regard, claim 1 defines "***logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a remaining portion of the system bus not included in the first portion, wherein the logic capable of being configured to interface with the first portion of the system bus is operatively connected with the logic capable of being configured to interface with the companion integrated circuit.***" No such comparable teaching or feature is disclosed in the'906 patent.

Simply stated, there is no teaching in the '906 patent of a single integrated circuit having logic for interfacing with a first portion of a system bus (the first portion being less than all of the system bus) and second logic for interfacing with a companion integrated circuit to receive information communicated over a second portion of the system bus. As

claims 2-10 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons.

With regard to independent claim 11, claim 11 recites:

> 11. A system comprising:
> a plurality of companion integrated circuit components that collectively implement a logic function embodied in a single, conventional integrated circuit component, ***each companion integrated circuit component comprising***:
> a first logic interface for communicating with a remote component via ***a portion of a system bus, wherein the portion of the system bus comprises only approximately half of a set of signal lines that comprise a the system bus;***
> ***a second logic interface for communication with a companion logic interface of a remaining one of the plurality of the integrated circuit components over a separate bus, wherein the first logic interface is operatively connected with the second logic interface***; and
> logic for controlling the selective communication of information received by the first logic interface via the portion of the system bus through the second logic interface to the companion integrated circuit.

(*Emphasis added*). Applicants respectfully submit that claim 11 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

Like the rejection of claim 1, the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as comprising the claimed second logic interface. This rejection simply makes no sense, in the context of the claimed embodiments.

In this regard, the first logic interface is specifically claimed as "communicating with a remote component via a portion of a system bus." In contrast, the second logic interface

is specifically claimed as being configured for "communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus." This is not taught or disclosed in the '906 patent. In fact, the only input to the applied I/O register 671 is bit positions D[0:7] of the data bus 680. These bit positions couple to I/O register 671 at reference number 682. Significantly, the register 671 cannot comprise the claimed second logic interface, assuming that that register 671 comprises the first logic interface. Furthermore, the I/O registers 671 and 673 are disposed in separate integrated circuit chips, so these elements cannot be mixed and matched as applying to the first and second logic interfaces, as claim 11 requires that the first and second logic interfaces be in a single integrated circuit component.

For at least these reasons, the rejections of claim 11 should be withdrawn.

With regard to claim 20, independent claim 20 recites:

> 20. An integrated circuit component comprising:
> a first set of conductive pins for channeling communications with a remote component via only a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal lines that make up a system bus, but not all of the signal lines that make up the system bus;
> a second set of conductive pins for channeling communications with a companion integrated circuit component;
> additional conductive pins for carrying additional control and communication signals;
> wherein collectively, the conductive pins of the integrated circuit component do not directly accommodate all signal lines of the system bus, but rather directly accommodate fewer than all of the signal lines of the system bus.

The Office Action essentially copied the rejection of claim 1 and pasted it in the remarks section with respect the rejection of claim 20. In this regard, the Office Action referred to a "first logic interface" (see p. 11, line 9), even though no such element exists in claim 20.

In addition to the rejections copied from claim 1, the Office Action further concluded that "it is inherent that pins must be provided for connections between discrete chips or ICs." (see Office Action, p. 11, last three lines). Finally, the Office Action alleged (Office Action, top of p. 12) that "the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component." In essence, the rejection of claim 20 appears to take the position that the recited features are inherent in the structure recited in claims 1 or 11, and then relies on the rejections of those claims. In response, Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11. For the same reasons, the rejection of claim 20 should be withdrawn.

As the remaining claims depend from either claim 1, 11, or 20, all remaining claims 2-10, 12-19, and 21-24 patently define over the cited art.

DUTY OF DISCLOSURE

With regard to the "duty of disclosure" issue raised by the Examiner, Applicants fully addressed this issue in Applicants' previous response. In the present Office Action, the Examiner states: "it is still this Examiner's position that Application No. 10/630,260

and this application (10/630,460) are not only related but also directed to the same subject matter." Applicant disagrees, particularly in view of the current state of the claims in each of these applications. With all due respect to the Examiner, it was the undersigned who initially interviewed these applications with the inventors, it was the undersigned who drafted these applications, and it is the undersigned who has the best understanding of the relevant subject matter of these applications, and the focus of their respective claims.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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